LOW NOISE AMPLIFIERS USING TWO DIMENSIONAL ELECTRON GAS FETS

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Abstract

Recently developed LNAs incorporating two dimensional electron gas (2 DEG) FETs for satellite communications earth stations are disclosed, which give epoch-making low noise as FET LNAs to operate in the 2, 4, 12, and 20 GHz bands at room temperature, especially under cooled state. Typically detailed further is newly developed 4 GHz band LNA with 55 K max. noise temperature at room temperature, noise temperatures of the order of 30 K across 800 MHz bandwidth (3.4 to 4.2 GHz) under thermoelectrically (TE-) cooled state (about-45°C), which has been adopted in the new earth station conducted by KDD.

Introduction

Present-day satellite communications LNAs fall in two categories: the parametric LNA and the FET LNA. As a recent trend, much lower noise temperature and broader frequency band (to meet INTELSAT X'pole compensation and WARC 79 recommendations) have become essential for INTELSAT application, while maintenance-free benefits have been called for DOMSAT application with increasing number of small earth stations operated worldwide. The former is essentially superior in noise performance, but requires complex maintenance service and is expensive. In contrast, the latter features ease of handling, compactness, and lower cost [1].

This is the reason why the realization of noise performance of the FET LNAs well comparable with the parametric LNAs has been eagerly pursued. To meet these requirements, our research and developmental efforts have been directed to the 2 DEG FET to have high potentiality as an ultra-low-noise device as well as to the low-loss and broadband noise matching technologies for an input circuit to be installed ahead of the 2 DEG FET. As a result, 2 DEG FET LNAs having ultra-low-noise characteristics in the four frequency bands (2, 4, 12, and 20 GHz) were successfully developed.

Device Structure and Performance

By 2 DEG FET is meant a device utilizing a hetero-junction between Si-doped AlGaAs and undoped GaAs to advantage, whose basic structure is shown in Fig.1 [2]. With this structure, the AlGaAs side donor region and the GaAs side two dimensional electron channel can be spatially separated each other.

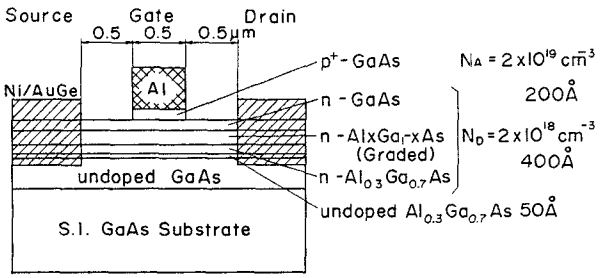

Fig. 1 Structure of the 2 DEG FET.

As a result, the two dimensional electron gas flowing along the channel formed in the high-purity GaAs region will be less susceptible to the scattering effect caused by impurities, or donors, to attain electron mobility as high as 1.5 times the values of conventional GaAs FETs at room temperature. Since it can be experimentally verified that improvements in electron mobility are pronounced under cooling state, practical application and advantages of 2 DEG FET as an ultra-low-noise device had been eagerly sought.

At present, the excellent microwave characteristics as will be described have been experimentally achieved with 2 DEG FET alone.

The noise temperature (NT) and gain vs frequency characteristics, of 2 DEG FET are shown in Fig.2. This data is calculated from the NT and gain data measured at various frequencies under room temperature conditions using the circuit of Fig.3, account being taken of losses in various circuit portions and the gain of 2 DEG FET. As obvious from Fig.2, ultra-low-noise and high-gain properties of the 2 DEG FET far surpassing the conventional GaAs FETs are secured even at room temperature.

Further, the manner in which the NT is improved by cooling 2 DEG FET with the gaseous helium refrigerator suitable for tests in a wide cooling range and the cooling circuit structure shown in Fig.4 will be described. Fig.5 illustrates the ambient-temperature-dependent NT characteristics of the 2, 4, 12, and 20 GHz 2 DEG FETs per se, respectively. These data are calculated from the

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experimental NT data obtained at 2, 4, 12, and 20 GHz under cooled state, account being taken of cooling circuit losses and the gain of the 2 DEG FET.

The NT vs ambient temperature relationships of the FETs [1], [3] can be generally expressed as

$$\frac{Te2}{Te1} = \left(\frac{Td2}{Td1}\right)^{x} \quad \ldots\ldots (1)$$

where

Te1 = NT of 2 DEG FET at room temperature,
Te2 = NT of 2 DEG FET under cooled state,
Td1 = room temperature,
Td2 = cooling temperature,
x = noise reduction factor.

An analysis of data taken from the graph of Fig.5 demonstrates that noise reduction factor x due to cooling of 2 DEG FET becomes more than about 1.7, apparently higher than x = 1.5 of the conventional GaAs FETs. That is, the degree of improvement in noise performance caused by cooling is more pronounced over the conventional GaAs FETs.

The 2 DEG FET featuring ultra-low-noise and high gain properties has been adopted this time as the preamplifier stage of the LNA, which plays a dominant role for reduction of overall noise. That the preamplifier stage has such properties should be extremely advantageous in noise reduction especially when the LNA constitutes a multi-stage amplifier.

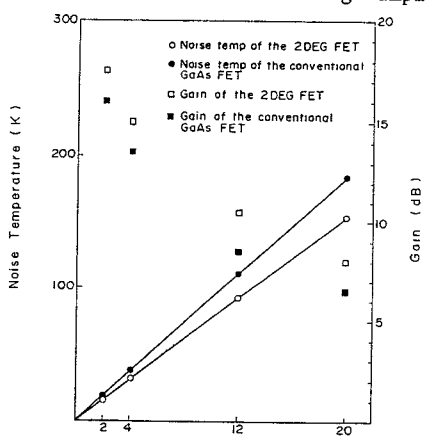


Fig 2 Noise temperature and gain of the 2 DEG FET proper as a function of frequency.

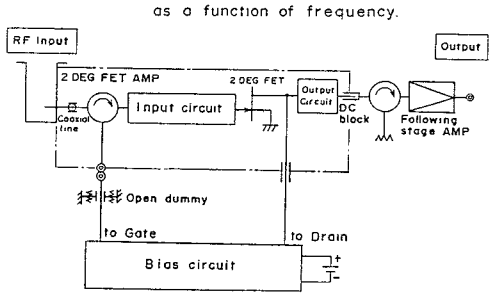


Fig.3 Circuit structure used in measuring performance data of the 2 DEG FET at room temperature.

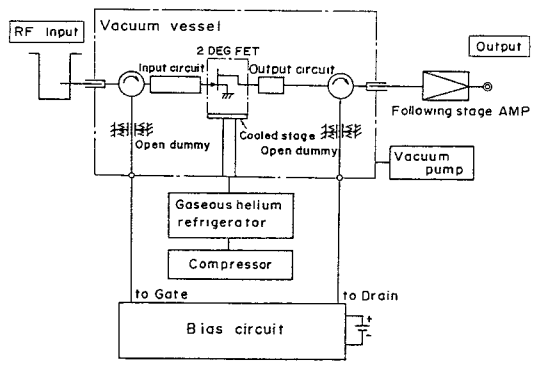


Fig 4 Circuit configuration used for experiment of cooled temperature dependence of the 2 DEG FET,s noise temperature.

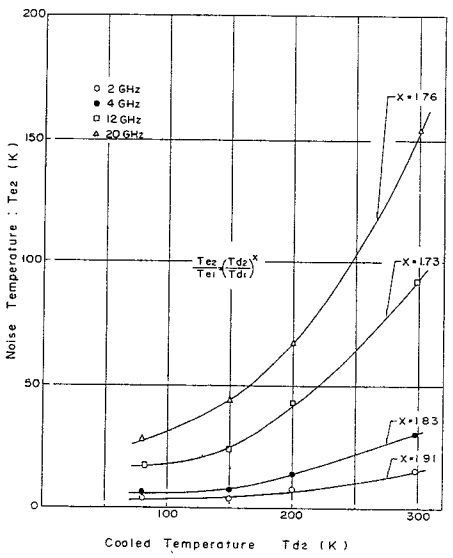


Fig 5 Cooled temperature dependence of noise temperature of the 2 DEG FET at 2, 4, 12 and 20 GHz.

LNA's Circuit Design

Design knowledge for the preamplifier stage incorporating 2 DEG FET will now be analyzed. Where a lossless impedance matching circuit is connected to the input of an FET, the noise figure (NF) of the amplifier is dependent upon the output impedance of the input circuit [4] and is given by:

$$F = Fmin + \frac{Rn}{Gs}\{(Gs - Go)^2 + (Bs - Bo)^2\} \quad \ldots (2)$$

where

F = NF determined by input circuit,
Fmin = optimum NF,
Rn = equivalent input noise resistance.

Here, the admittance (Yo) to give optimum NF and the source admittance (Ys) of the input circuit can be respectively expressed as

$$Yo = Go + jBo \quad \ldots\ldots (3)$$
$$Ys = Gs + jBs \quad \ldots\ldots (4)$$

As obvious from eq. (1), to construct the FET preamplifier stage to give optimum NT, it is desirable that the input side impedance be coincident with the optimum impedance for noise reduction as decided by the 2 DEG FET (Yo = Ys). Incidentally, the locus of calculated noise optimum impedances as plotted on the smith chart will invariably be inside of S_{11}* as in Fig.6. Need arises, therefore, for inserting an isolator on the input side of the 2 DEG FET, because the degradation in the input VSWR of the FET is inevitable to secure an optimum impedance match for noise reduction. Where a suitable circuit is placed on the input side of an FET, the loss in the circuit will cause the degradation in noise performance of an amplifier. Consequently, in order for potentiality of the 2 DEG FET to be maximally displayed, it is essential that an extremely low-loss circuit capable of maintaining noise optimum impedance matching over a wide frequency band be connected between the input isolator and the 2 DEG FET as the preamplifier stage input circuit configuration.

Furthermore, an impedance-matching circuit, as the output circuit, for transforming the input impedance S_{22}* into 50 ohms at the output port must be installed in order to lessen the effect of NT of the subsequent stages by maximizing the gain of the preamplifier stage.

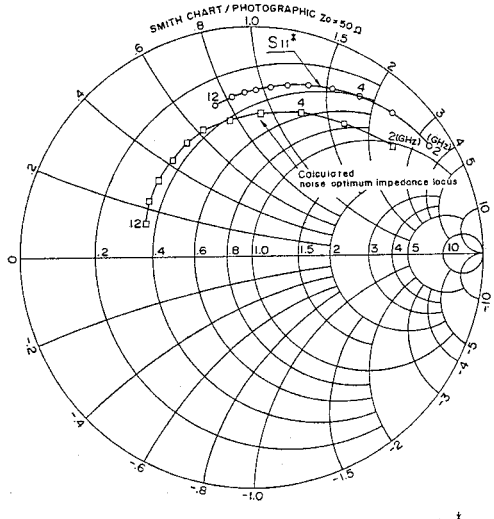
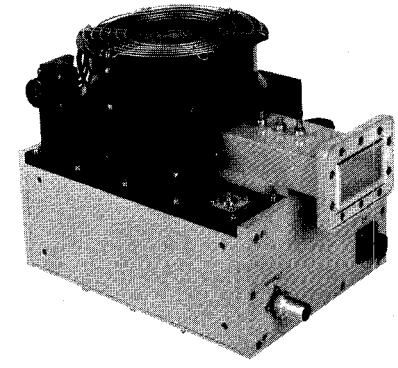


Fig.6 Noise optimum impedance locus and S_{11}* of the 2 DEG FET.

Fig.7 shows a photo and a block diagram of the newly developed 4 GHz TE-cooled 2 DEG FET LNA as a typical example of a circuit structure involving the low-loss and noise matched circuit and the 2 DEG FET. Among the innovative concepts adopted in the design of the newly developed preamplifier stage input circuit are:

First, transformation of the impedance at the output port of the isolator's stripline is effected, for taking noise optimum impedance matching, by use only of the triplate type λ/2-line-length resonator and the FET's lead inductance. This has brought about a marked reduction of the insertion loss over conventional matching circuits.

Second, favorable noise matching can be taken with ease over as wide a bandwidth as 800 MHz due to the λ/2 resonator's effect, as opposed to conventional preamplifier stage.



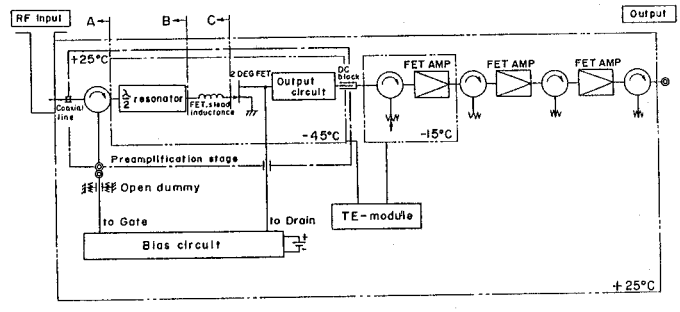


Fig.7. 4GHz TE-cooled 2 DEG FET LNA and the block diagram.

The manner in which the loci formed by plotting impedances at various points in the input matching circuit on the smith chart for optimum noise matching vary from one another by the impedance transformation process is illustrated in Fig.8. A comparison between locus C for the impedance of the input circuit ahead of the 2 DEG FET as looked into the RF input side at C in Fig.7 and noise optimum impedance locus D reveals at once that they are arranged in the same H-L direction and approximately the same in arc length. Thus, combining newly developed input matching circuit and 2 DEG FET has enabled feasibility of the preamplifier stage with excessively low noise over a wide frequency band.

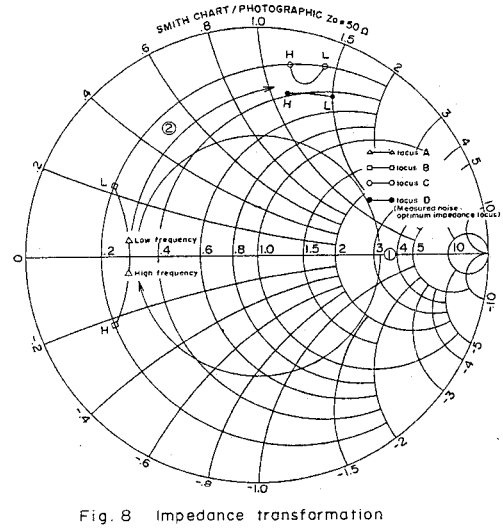


Fig. 8 Impedance transformation for taking optimum noise matching.

As to the bias circuit, two design precautions must be taken:

(1) Since the optimum bias voltage for the 2 DEG FET is extremely low, the bias circuit must be designed to meet this condition.

(2) The bias circuit must incorporate a protective circuit against incoming surge voltages.

Fig.9 shows a block diagram used for computation of overall NT of the 4 GHz LNA incorporating the newly developed input matching circuit at room temperature and under TE-cooled state (-45°C), and various formula used for noise budget computations. Incidentally, NT of 2 DEG FET alone under TE-cooled state is calculated using noise reduction factor x = 1.83 at 4 GHz derived by an analysis of the ambient-temperature-dependant graph of Fig.5. The noise budget in Fig.9 theoretically predicts feasibility of an LNA with NT of 47 K at room temperature and NT of 34 K under TE-cooled state.

Block diagram	Noise temp gain/loss	Formula at input	at room temp (+25°C) Te/G/Te/L	at room temp (+25°C) Noise temp at input	under TE-cooled state (-45°C) Te/G/Te/L	under TE-cooled state (-45°C) Noise temp at input
WG/Coax transition	Loss L1 (Te1)	$(L_1-1)\,T_{e1}$	L1=0.05dB Te1=298K	3.45 K	L1=0.05dB Te1=298K	3.45 K
Coaxial line	Loss L2 (Te2)	$L_1L_2\,T_{e2}\,(1-\frac{1}{L_2})$	L2=0.01dB Te2=298K	0.69 K	L2=0.01dB Te2=298K	0.69 K
Isolator	Loss L3 (Te3)	$L_1L_2L_3\,T_{e3}\,(1-\frac{1}{L_3})$	L3=0.09dB Te3=298K	6.33 K	L3=0.09dB Te3=298K	6.33 K
λ/2-line-length resonator	Loss L4 (Te4)	$L_1L_2L_3L_4T_{e4}(1-\frac{1}{L_4})$	L4=0.03dB Te4=298K	2.14 K	L4=0.03dB Te4=228K	1.64 K
2 DEG FET	Noise Te1 Gain G1 (Te2)	$L_1L_2L_3L_4\,T_{e1}$	Te1=307.5K G1=15dB Te2=298K	32.06 K	Te1=118.84K G1=15dB Te2=228K	19.64 K
Output circuit	Loss L5 (Te5)	$\frac{L_1L_2L_3L_4L_5\,T_{e5}}{G_1}(1-\frac{1}{L_5})$	L5=0.05dB Te5=298	0.11K	L5=0.05dB Te5=228K	0.09 K
DC block	Loss L6 (Te7)	$\frac{L_1L_2L_3L_4L_5L_6\,T_{e7}}{G_1}(1-\frac{1}{L_6})$	L6=0.1dB Te7=298K	0.23K	L6=0.1dB Te7=228K	0.18K
Following stage	Noise Te2	$\frac{L_1L_2L_3L_4L_5L_6\,T_{e2}}{G_1}$	Te2=650K	2.05K	Te2=51K	1.74K
Overall noise temp Te	$T_e=(L_1-1)T_{e1}+L_1L_2\,T_{e2}(1-\frac{1}{L_2})$ $+L_1L_2L_3\,T_{e3}(1-\frac{1}{L_3})$ $+L_1L_2L_3L_4\,T_{e4}(1-\frac{1}{L_4})$ $+L_1L_2L_3L_4\,T_{e1}$ $+\frac{L_1L_2L_3L_4L_5\,T_{e5}}{G_1}(1-\frac{1}{L_5})$ $+\frac{L_1L_2L_3L_4L_5L_6\,T_{e7}}{G_1}(1-\frac{1}{L_6})$ $+\frac{L_1L_2L_3L_4L_5L_6\,T_{e2}}{G_1}$		47.06K		33.76K	

Fig 9 Noise budget of 4 GHz TE-cooled 2 DEG FET LNA.

Experimental Data Summary

Typical data measured at room temperature and under TE-cooled state of the overall noise characteristics of the newly developed 4 GHz band 2 DEG FET LNA shown in Fig.7 are illustrated in Fig.10. From these measured data, the noise temperature at 4 GHz is known to be 48.7 K at room temperature and 36 K under TE-cooled state. These values compare favorably with the theoretically predicted values indicated in Fig.9.

Furthermore, noise temperatures on the order of 30 K, 34 to 39.6 to be exact, unprecedentedly low values which could never be attained so far with conventional TE-cooled FET LNAs, were obtained with the LNA shown in Fig.7 over a wide frequency band of 800 MHz under TE-cooled state. This data is undoubtedly the lowest of all values reported so far of the conventional TE-cooled type FET LNAs.

Conclusion

Integrating the two approaches—ultra-low-noise property of 2 DEG FET and LNA technology, has brought about a success with the development of 2 DEG FET LNAs featuring superior noise characteristics in the 2, 4, 12, and 20 GHz bands. Incidentally, the newly developed 4 GHz TE-cooled 2 DEG FET LNA detailed as a typical example is designed to meet the specification of INTELSAT Standard-A earth station across 800 MHz bandwidth sufficiently.

The trend toward wider bandwidth and lower noise temperature will be further accelerated hereafter with the advancement of circuit, ferrite device, and cooling technologies and the improvement of the characteristics of the 2 DEG FET per se. The authors are convinced that the advent of the satellite communications FET LNAs superior in performance to the parametric LNAs can be expected before long.

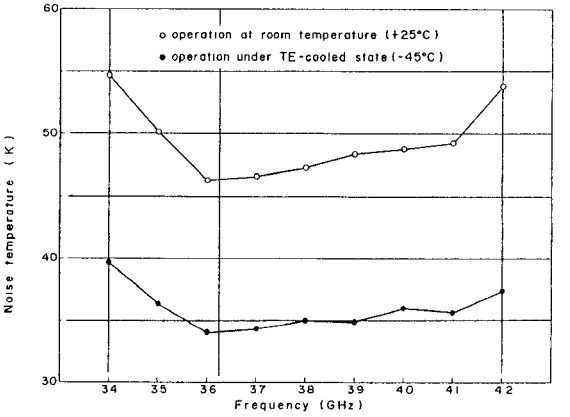


Fig 10 Typical noise performance data taken from 4GHz band TE-cooled 2 DEG FET LNA

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